FORM PTO-1390 (REV 11-2000)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 124-889
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5) 09/936561
INTERNATIONAL APPLICATION NO. **PCT/GB00/00953**	INTERNATIONAL FILING DATE **15 March 2000**	PRIORITY DATE CLAIMED **17 March 1999**

TITLE OF INVENTION

ELECTROMAGNETIC WAVE RECEIVER FRONT END

APPLICANT(S) FOR DO/EO/US

MUNDAY et al

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☐ The U.S. has been elected by the expiration of 19 months from the priority date (Article 31).
5. A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has **NOT** expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 To 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☐ Other items or information.

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1 5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/936561	PCT/GB00/00953	124-889

21. ☒ The following fees are submitted:

	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5):	
-- Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00	
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $860.00	
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO $710.00	
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $690.00	
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00	

ENTER APPROPRIATE BASIC FEE AMOUNT =						$	860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).						$	130.00	
CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE				
Total Claims	33	-20 =	13	X	$18.00	$	234.00	
Independent Claims	8	-3 =	5	X	$80.00		400.00	
MULTIPLE DEPENDENT CLAIMS(S) (if applicable)					$270.00	$	0.00	
TOTAL OF ABOVE CALCULATIONS =						$	**1624.00**	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.							0.00	
SUBTOTAL =						$	**1624.00**	
Processing fee of $130.00, for furnishing the English Translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)). +							0.00	
TOTAL NATIONAL FEE =						$	**1624.00**	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). **$40.00** per property +						$	0.00	
Fee for Petition to Revive Unintentionally Abandoned Application ($1240.00 – Small Entity = $620.00)						$	0.00	
TOTAL FEES ENCLOSED =						$	**1624.00**	
						Amount to be: refunded	$	
						Charged	$	

a. ☒ A check in the amount of $1624.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 14-1140 in the amount of $_____ to cover the above fees. A duplicate copy of this form is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-1140. A duplicate copy of this form is enclosed.
d. ☒ The entire content of the foreign application(s), referred to in this application is/are hereby incorporated by reference in this application.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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Stanley C. Spooner
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27,393 REGISTRATION NUMBER

September 14, 2001 Date

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

MUNDAY et al — Atty. Ref.: 124-889

National Phase of Int'l Appln. No. PCT/GB00/00953 — Group:

(Filed: 15 March 2000) — Examiner:

For: ELECTROMAGNETIC WAVE RECEIVER FRONT END

* * * * * * * * * * *

September 14, 2001

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

Please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel without prejudice claims 1 – 24 and enter newly written claims 25-57 as follows:

25. *(New)* A receiver front end capable of receiving electromagnetic wave signals having frequencies in the range of substantially 35GHz to substantially 40GHz, and having a gain of substantially 24dB or above and a noise figure of substantially 4dB or below, and comprising at least one multifunction monolithic microwave integrated circuit (MMIC).

26. *(New)* A receiver front end according to claim 25 which has a noise figure of substantially 4dB or below over an output signal frequency range of substantially 1 to 10GHz.

27. *(New)* A receiver front end according to claim 25 wherein the or each multifunction receiver front end MMIC has at least one of the following components:

(i) an EM wave amplifier adapted to amplify the electromagnetic wave signals received by the MMIC;

(ii) a filter adapted to filter the electromagnetic wave signals received by the MMIC;

(iii) a frequency converter adapted to convert the frequency or frequencies of the electromagnetic wave signals to a lower or higher frequency or frequencies;

(iv) a converted-signal amplifier adapted to amplify the converted signals.

28. *(New)* A receiver front end according to claim 27 wherein at least two of (i) to (iv) are provided on the same chip.

29. *(New)* A receiver front end according to claim 27 wherein at least three of (i) to (iv) are provided on the same chip.

30. *(New)* A receiver front end according to claim 27 wherein all four of (i) to (iv) are provided on the same chip.

31. *(New)* A receiver front end according to claim 30 which comprises a receiver MMIC and a doubler/buffer amplifier MMIC, and in which said receiver MMIC comprises a low noise amplifier (LNA), with a noise figure less than 4dB.

32. *(New)* A receiver front end according to claim 31 wherein said LNA is a balanced amplifier having separate amplification sections, and each electromagnetic signal received by said LNA is split into two substantially symmetric signals, each of which is fed into said separate amplification sections.

33. *(New)* A receiver front end according to claim 32 wherein each said amplification section has three stages of amplification, and the output of each said amplification section is combined, and the combined signal output from said LNA.

34. *(New)* A receiver front end according to claim 32 wherein said receiver MMIC comprises a mixer, and in which said mixer is adapted to convert the frequency of a signal output from the LNA to a lower frequency mixer output signal.

35. *(New)* A receiver front end according to claim 34 in which said mixer comprises two diodes and the signal from said LNA is fed into said diodes along with a reference signal and said diodes are adapted to multiply the signal from said LNA and said reference signal and output an output signal having a frequency equal to the difference in frequency of the signal from said LNA and the frequency of said reference signal.

36. *(New)* A receiver front end according to claim 35 wherein said mixer is a 90° balanced mixer.

37. *(New)* A receiver front end according to claim 34 wherein said receiver MMIC comprises a filter, and said filter is disposed between said LNA and said mixer, to filter the signal from said LNA before it is fed to said mixer, and wherein the passband of said filter is such that it suppresses a sideband of the signal from said LNA.

38. *(New)* A receiver front end according to claim 37 wherein said filter comprises a distributed transmission line and wherein said filter is folded into a serpentine layout.

39. *(New)* A receiver front end according to claim 31 wherein said receiver MMIC comprises an IF amplifier, and the IF amplifier is adapted to receive an IF output signal from said mixer and to amplify it to produce an IF output signal which is output from said receiver MMIC, and wherein said amplifier comprises a single transistor stage having gate and drain

terminals, and in which a parallel resistor-inductor-capacitor feedback network is applied between said gate and drain terminals of said transistor.

40. *(New)* A receiver front end according to claim 34 wherein said doubler/buffer amplifier MMIC is placed between a local oscillator, adapted to produce said reference signal, and said mixer, and the doubler/buffer amplifier MMIC receives said reference signal produced by said local oscillator and doubles the frequency of this signal producing a new reference signal which is fed to said mixer.

41. *(New)* A receiver front end according to claim 40 wherein said doubler/buffer amplifier MMIC comprises a filter component comprising two quarter wavelength open circuit stubs.

42. *(New)* A receiver front end package comprising a receiver front end according to claim 25, power supply components for said receiver front end, and connectors for said receiver and said power supply components.

43. *(New)* A receiver front end package according to claim 42 which is double sided with separate enclosures and provides isolation of said electromagnetic wave receiver front end and said power supply components into the separate enclosures, and in which connections are made between said receiver front end and said power supply components using glass bead feedthroughs in said package.

44. *(New)* A receiver front end package according to claim 42 having voltage bias lines wherein said power supply components comprise DC biasing circuits on a circuit board, and in which said biasing circuits contain bias sequencing and voltage regulation for all of the bias lines of said receiver front end.

45. *(New)* A receiver front end package according to claim 44 wherein said connectors are connected to the receiver front end using an airline launch technique with a better than 20dB impedance match of said connectors with said receiver front end.

46. *(New)* A receiver front end package according to claim 42 wherein said receiver front end package is connected to an antenna which detects the electromagnetic waves, and is bodily movable with said antenna.

47. *(New)* A receiver front end package according to claim 46 in which said receiver front end package is mounted on said antenna or a movable component thereof and can move with said antenna or component.

48. *(New)* A phased array system comprising a plurality of receiver front ends according to claim 25.

49. *(New)* A high data rate communications system comprising one or more receiver front ends according to claim 25.

50. *(New)* A receiver front end comprising:

i) a first amplifier adapted to amplify a received signal and provide an amplified signal;

ii) a filter adapted to filter said amplified signal and provide a filtered signal;

iii) a mixer adapted to take a reference signal and said filtered signal and mix them such that said mixer provides an output in a frequency range different from that of said filtered signal, so as to provide a mixed signal;

iv) a second amplifier adapted to amplify said mixed signal.

51. *(New)* A receiver front end comprising:

i) a first amplifier adapted to amplify a received signal and provide an amplified signal;

ii) a filter adapted to filter said amplified signal and provide a filtered signal;

iii) a mixer adapted to take a reference signal and said filtered signal and mix them such that said mixer provides an output in a frequency range different from that of said filtered signal, so as to provide a mixed signal;

iv) a second amplifier adapted to amplify said mixed signal; and

wherein the first amplifier comprises:

a) a first Lange coupler adapted to split the signal in first and second signals such that said first and second signals have substantially 90° phase difference;

b) a first amplification section adapted to amplify said first signal and a second amplification section adapted to amplify said second signal, said first and second amplification sections having balanced topographies, each section having first, second and third transistors and a gate and a drain bias for said transistors, said gate and drain biases being common to all the transistors; shunt resistors associated with the gate of each transistor; a series resistor-inductor-capacitor network in parallel with said section; and parallel feedback being provided across said third transistor; and

c) said first and second stages having respective outputs, and a further Lange coupler being provided so as to combine said outputs of said amplification sections.

52. *(New)* A receiver front end comprising:

i) a first amplifier adapted to amplify a received signal and provide an amplified signal;

ii) a filter adapted to filter said amplified signal and provide a filtered signal;

iii) a mixer adapted to take a reference signal and said filtered signal and mix them such that said mixer provides an output in a frequency range different from that of said filtered signal, so as to provide a mixed signal;

iv) a second amplifier adapted to amplify said mixed signal; and

wherein said mixer comprises:

a) a Lange coupler arranged such that both said reference signal and said filtered signal are added together and then separated into first and second signals with a phase difference of substantially 90°; and

b) first and second diodes, each supplied with one of said phase separated first and second signals, said first and second diodes being arranged such that said first diode is in one orientation with respect to said first input signal and said second diode is in the opposite orientation with respect to said second signal;

and arranged such that a combined output signal of said first and second diodes has a frequency substantially equal to the difference between said reference and filtered signals.

53. *(New)* A receiver front end comprising:

i) a first amplifier adapted to amplify a received signal and provide an amplified signal;

ii) a filter adapted to filter said amplified signal and provide a filtered signal;

iii) a mixer adapted to take a reference signal and said filtered signal and mix them such that said mixer provides an output in a frequency range different from that of said filtered signal, so as to provide a mixed signal;

iv) a second amplifier adapted to amplify said mixed signal; and

wherein said filter is a distributed transmission line filter, arranged in a serpentine fashion, containing quarter wave coupled elements, said filter being adapted to suppress a sideband of the output of said first amplifier.

54. *(New)* A receiver front end according to claim 53 wherein said filter is adapted to have a passband of substantially 35 GHz to substantially 40 GHz.

55. *(New)* A receiver front end comprising:

i) a first amplifier adapted to amplify a received signal and provide an amplified signal;

ii) a filter adapted to filter said amplified signal and provide a filtered signal;

iii) a mixer adapted to take a reference signal and said filtered signal and mix them such that said mixer provides an output in a frequency range different from that of said filtered signal, so as to provide a mixed signal;

iv) a second amplifier adapted to amplify said mixed signal; and

wherein said second amplifier has an output impedance and comprises a single transistor having a gate and a drain bias, a resistor-inductor-capacitor network provided between gate and drain terminals of said transistor and a resistor-capacitor network adapted to match said input impedance of the second amplifier to that required by said mixer for proper operation thereof.

56. *(New)* A receiver front end comprising:

i) a first amplifier adapted to amplify a received signal and provide an amplified signal;

ii) a filter adapted to filter said amplified signal and provide a filtered signal;

iii) a mixer adapted to take a reference signal and said filtered signal and mix them such that said mixer provides an output in a frequency range different from that of said filtered signal, so as to provide a mixed signal;

iv) a second amplifier adapted to amplify said mixed signal; and

wherein said reference signal is generated by means of a local oscillator, the output of which is used to supply a frequency doubler, the output of said doubler being passed through an amplifier before being used as said reference signal.

57. *(New)* A receiver front end comprising:

i) a first amplifier adapted to amplify a received signal and provide an amplified signal;

ii) a filter adapted to filter said amplified signal and provide a filtered signal;

iii) a mixer adapted to take a reference signal and said filtered signal and mix them such that said mixer provides an output in a frequency range different from that of said filtered signal, so as to provide a mixed signal;

iv) a second amplifier adapted to amplify said mixed signal; and

wherein the first amplifier comprises:

a) a first Lange coupler adapted to split the signal in first and second signals such that said first and second signals have substantially 90° phase difference;

b) a first amplification section adapted to amplify said first signal and a second amplification section adapted to amplify said second signal, said first and second amplification sections having balanced topographies, each section having first, second and third transistors

and a gate and a drain bias for said transistors, said gate and drain biases being common to all the transistors; shunt resistors associated with the gate of each transistor; a series resistor-inductor-capacitor network in parallel with said section, and parallel feedback being provided across said third transistor; and

c) said first and second stages having respective outputs, and a further Lange coupler being provided so as to combine said outputs of said amplification sections; and

wherein said mixer comprises:

a) a Lange coupler arranged such that both said reference signal and said filtered signal are added together and then separated into first and second signals with a phase difference of substantially 90°; and

b) first and second diodes, each supplied with one of said phase separated first and second signals, said first and second diodes being arranged such that said first diode is in one orientation with respect to said first input signal and said second diode is in the opposite orientation with respect to said second signal;

and arranged such that a combined output signal of said first and second diodes has a frequency substantially equal to the difference between said reference and filtered signals; and

wherein said filter is a distributed transmission line filter, arranged in a serpentine fashion, containing quarter wave coupled elements, said filter being adapted to suppress a sideband of the output of said first amplifier;

wherein said second amplifier has an output impedance and comprises a single transistor having a gate and a drain bias, a resistor-inductor-capacitor network provided between gate and drain terminals of said transistor and a resistor-capacitor network adapted to match said input impedance of the second amplifier to that required by said mixer for proper operation thereof; and

wherein said reference signal is generated by means of a local oscillator, the output of which is sued to supply a frequency doubler, the output of said doubler being passed through an amplifier before being used as said reference signal.

REMARKS

The above amendments are made to place the claims in a more traditional format.

Respectfully submitted,

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09/936124

ELECTROMAGNETIC WAVE RECEIVER FRONT END

This invention relates to improvements in electromagnetic wave receiver front ends capable of receiving waves having frequencies in the radio frequency range, and the components used therefor.

In recent years there has been a tremendous growth in the number of applications where it is desirable to be able to receive electromagnetic waves having frequencies in the radio frequency range, and particularly in the range of ten's of gigahertz (i.e. having wavelengths of millimeters, called mm-wave frequencies). Such applications include local multipoint distribution systems (LMDS), microwave video on demand systems (MVDS), collision avoidance radar, wireless local area networks (WLANs) and others. This trend is further driven by increasing frequency spectrum congestion at lower (microwave) frequencies, and the desire to have global communications with ever increasing data rates. For mm-wavelength receiver technology to be successful in the market place, it is important that acceptable performance is achieved while, at the same time, component size and cost is minimised. This is so for all components of such receivers including receiver front end components which generally receive electromagnetic wave signals from, for example, an antenna and process these signals before passing them to further receiver components.

According to a first aspect of the present invention, there is provided a receiver front end capable of receiving electromagnetic wave signals having frequencies in the range of substantially 35GHz to substantially 40GHz, and having a gain of substantially 24dB or above and a noise figure of substantially 4dB or below, and comprising one or more multifunction monolithic microwave integrated circuits (MMICs).

The receiver front end preferably has a noise figure of substantially 4dB or below. This is preferably over an output signal frequency range of substantially 1 to 10GHz, and preferably at least over substantially 2 to substantially 8 GHz. Prior art receivers based on similar technology typically have noise figures of greater than or equal to 6dB at such frequencies i.e. mm-wave frequencies.

The receiver front end preferably has a size in the region of $30mm^2$, or less than this for example $28mm^2$ or $25mm^2$. The small size of the receiver front end is particularly useful for applications where a multiple of receiver front ends are required to be placed close together in a small space.

The or each receiver front end MMIC may have a GaAs substrate. MMICs are a key enabling technology for mm-wavelength receivers due to their small size, improved reliability, high repeatability and the potential for low cost. Multifunction MMICs, integrating several functions onto a single MMIC, are particularly attractive since they allow further size, weight and reliability improvements arising from the use of fewer MMICs. The low cost and low parts count of multifunction MMICs makes the receiver front ends incorporating such MMICs easily replaceable if they fail.

The or each multifunction receiver front end MMIC may carry out a plurality of functions or two or more functions, or three or more functions, or preferably at least four functions. These functions may comprise amplification of the electromagnetic wave signals received by the MMIC, and/or filtering the electromagnetic wave signals, and/or conversion of the frequency or frequencies of the electromagnetic wave signals to a lower or higher frequency or frequencies, and/or amplification of the converted signals.

When multiple single function MMICs are used in a receiver front end, connections, such as tape bonds, bond wires or flip MMIC connections, need to

be provided between these. At each connection there is the possibility of the introduction of interface parasitics into the signal, and such connections tend to filter high frequency (i.e. ten's of gigahertz) signals which is undesirable. In addition, the connections have to be very short to be usable in practice. By using one or more multifunction MMICs the number of MMICs required in an equivalent receiver front end is reduced, thereby reducing the number of connections required and the possibility of parasitics etc. In addition, when multiple of single function MMICs are used in a receiver front end, these may be manufactured from more than one semiconductor wafer and by more than one semiconductor manufacturing process. This may introduce differences in the operation of the MMICs due to differences in the semiconductor wafers or processing. When multifunction MMICs are used all of the functions may be included on the same wafer and on the same area of the wafer. This reduces the possibility of process differences between MMICs, and produces a smaller spread in performance characteristics than with the use of multiple single function MMICs.

The receiver front end preferably comprises a receiver MMIC and preferably a doubler/buffer amplifier MMIC.

The receiver MMIC may comprise a low noise amplifier (LNA). This is preferably the first component of the receiver front end and receives the electromagnetic wave signals. These signals may be received via microstrip transmission lines, or co-planar wave guides, or grounded co-planar wave guides. The LNA may be connected to one or more microstrip lines by 50μm gold tape bonds. The LNA preferably has a gain in the region of 24dB or, more preferably, greater than 24dB. The input and output port return losses are preferably greater than 12dB, and the noise figure preferably less than 4dB.

The LNA is preferably a balanced amplifier, and each electromagnetic signal

received by the LNA is preferably split into two substantially symmetric signals, each of which is fed into a separate amplification section. The two signals preferably have a 90° phase difference. Splitting of the signal improves the linearity of the operation of the LNA. Preferably a 90° coupler receives the electromagnetic signals and splits each of these into two signals. The coupler may be a Lange coupler.

It is important to have good impedance and power matching between the input of the receiver MMIC, i.e. the input of the LNA, and any circuit connected to this input for use (such as an antenna circuit). When a difference occurs between these impedances, a portion of the electromagnetic wave signals will be reflected at the input of the receiver MMIC. The receiver MMIC is preferably designed assuming that the impedance of any circuit connected to its input for use is 50Ω. This is a standard assumption in the design of such apparatus. The Lange coupler may comprise four ports. The first of these preferably receives the electromagnetic wave signals. The coupler splits these signals and produces two signals preferably output through the second and third ports. If imperfect impedance matching occurs at these ports some of the output signals will be reflected back through the coupler and out of the LNA. For proper operation, the Lange coupler is preferably provided with one or more resistive components, preferably on the fourth port of the coupler. These may comprise a load resistor of preferably 50Ω. Any signal reflected at the second and third ports is dissipated in this resistor and is not reflected out of the LNA of the receiver MMIC. The Lange coupler provides some decoupling of the receiver MMIC input impedance matching from variations in the impedance of the circuit connected to the receiver MMIC input. This is particularly important at frequencies of tens of gigahertz as small variations in the impedance of connections to the receiver MMIC input, such as tape bond connections, lead to a degraded noise figure performance.

Each amplification section of the LNA may use three stages of amplification. Three stages of amplification enables a gain specification of greater than 24dB to be met. It is important that the LNA has good gain characteristics as this minimises the effect of any noise contribution of the following components of the receiver MMIC. It is important that the noise introduced by the receiver front end and the receiver as a whole is as low as possible, as the receiver front end and the receiver are usually the first component in a chain of components and any noise introduced in the first component will be amplified by these other components.

Each stage of amplification may be provided with one or more transistors. Shunt resistors may be provided on each transistor gate. These provide low frequency stabilisation on each gate. Care is taken to ensure that the in-band noise figure is not degraded. A series resistor-inductor-capacitor network is preferably provided in parallel with the path of each split signal. This helps to overcome potential high frequency stability problems. Parallel feedback is preferably used across the third stage transistor. This helps to provide gain slope compensation and unconditional stability. All bias tracks, in both amplification sections, are preferably commoned so that only single gate and drain connections are required. This provides ease of use of the LNA. The output of each amplification section is combined, preferably using a Lange coupler, and the combined signal output from the LNA.

In a preferred embodiment, over the frequency range 30 to 40GHz the measured gain of the LNA is 23dB ± 1dB. The Lange couplers ensure that the input and output port return losses are better than 20dB. The LNA noise figure is approximately 3.2dB.

The receiver MMIC preferably further comprises a mixer. This preferably converts the frequency of the signal output from the LNA to a lower frequency

mixer output signal. The lower frequency signal is preferably output from the receiver MMIC to further stages of the receiver MMIC or to a component to which the receiver MMIC is attached for use. The frequency of the signal from the LNA is converted to a lower frequency signal, e.g. 5GHz (an intermediate frequency (IF)), as such signals can be more easily processed, unlike signals having frequencies greater than approximately 6GHz. The aim is to retain as much information in the signal from the LNA as possible, whilst reducing its frequency so that it can be more easily analysed.

The mixer preferably comprises two diodes. These may be positioned in the mixer back-to-back. Non-linear analysis may be used to determine the optimum diode size for mixer operation over a 30 to 45GHz frequency range. The signal from the LNA is preferably fed into the diodes along with a reference signal. The diodes preferably multiply the two signals, and, due to their non-linearity, output a signal having a frequency equal to the difference in frequency of the signal from the LNA and the frequency of the reference signal. If the frequency of the signal from the LNA is 35GHz and the frequency of the reference signal is 30GHz, then the frequency of the signal output from the mixer will be 5GHz. The reference signal is preferably provided by a local oscillator (LO). This may have a drive level of 13dBm.

The mixer may be a 90° balanced mixer. The reference signal from the LO and the signal from the LNA output are fed into input ports and are preferably split with a 90° phase difference preferably by a Lange coupler. One portion of each of the reference signal and the LNA signal is preferably fed to a first diode, and the other portions of these signals is preferably fed to the second diode which has its orientation reversed. Each diode preferably mixes the reference signals and the LNA signals and produces an IF output signal, which output signals are combined in phase and fed to an output port of the mixer. This 90° balanced mixer topology provides very good input and output port impedance matches,

giving the mixer input ports a broadband 50Ω impedance. In this topology, however, when the impedance matching of the diodes to the rest of the mixer is not ideal, some LNA signal may be reflected back out of the reference signal input port and some reference signal may be reflected back out of the LNA signal input port, i.e. the isolation of these ports, called LO-RF isolation, may be reduced. The mixer preferably has a conversion loss of less than 10dB. It preferably has LNA and reference signal input port return losses of greater than 15 dB. The LO-RF isolation may be greater than 6dB.

The above describes the situation when the signal from the LNA comprises only one frequency. This signal will more often comprise a range of frequencies. The mixer will then provide an output signal which has a range of frequencies, equal to the difference of the frequencies of the signal from the LNA and the frequency of the reference signal.

If the frequency of the reference signal is 30GHz, and the signal from the LNA comprises frequencies of 35GHz and 25GHz then both of these will result in an output of the mixer of 5GHz. The 35GHz and the 25GHz frequencies are referred to as upper and lower sidebands respectively. For many applications only one sideband, e.g. the upper sideband, is required to be converted by the mixer. This is called the wanted sideband. A filter can be used to filter out the unwanted sideband from the signal output from the LNA before it is fed to the mixer. The receiver is said to be capable of image rejection by suppressing a sideband, in this case the lower sideband.

The receiver MMIC preferably further comprises a filter. This is preferably placed between the LNA and the mixer, to filter the signal from the LNA before it is fed to the mixer. The passband of the filter is preferably such that it suppresses a sideband, preferably a lower sideband. The passband of the filter may be 35 to 40GHz, frequencies lying outside this band are said to lie in the

stopband of the filter. This will suppress a lower sideband of 25GHz, allowing only the 35GHz sideband to be output from the filter. The filter rejects the lower sideband, i.e. achieves image rejection.

The filter may comprise a distributed transmission line design. These are feasible when receiving waves of mm wavelengths, and do not require excessive MMIC area. Such a design is advantageous over lumped element filter designs at these wavelengths, which suffer from a relatively high insertion loss and are sensitive to process variations, particularly when metal-insulator-metal (MIM) capacitors are used. To reduce the receiver MMIC area the filter is preferably folded into a serpentine layout. A five element, quarter-wave coupled line filter may be used. This preferably produces a stopband attenuation of greater than 30dB, preferably 49dB, at 25GHz. The passband insertion loss of this filter is preferably in the region of 2.3dB from 35 to 40Ghz. The input and output port impedance matches are preferably better than 15dB.

The Lange coupler of the mixer preferably provides a 50Ω input impedance at the passband and stopband frequencies of the filter. This is essential to ensure that suppression of the frequencies in the stopband of the image rejection filter is not compromised.

The receiver MMIC preferably further comprises an IF amplifier. This preferably receives the IF output signal from the mixer and amplifies it producing an IF output signal which is output from the receiver MMIC. The majority of the amplification of the receiver as a whole is usually performed at intermediate frequencies in the IF amplifier, since gain blocks at these frequencies are relatively inexpensive.

The IF amplifier preferably comprises a single transistor stage. It preferably has a gain of greater than 9dB. A 400μm gate width transistor capable of delivering

15dBm of output power is preferably used for this amplifier. This avoids the IF amplifier compressing before the LNA. A parallel resistor-inductor-capacitor feedback network is preferably applied between the gate and drain terminals of the transistor. This helps to reduce the sensitivity of the IF amplifier to process variations. The IF amplifier input preferably presents a 50Ω impedance to the mixer at mm wavelengths as well as at IF frequencies. This helps to ensure correct mixer operation.

The receiver MMIC is preferably constructed from the building blocks described above. It is important during the design of the receiver MMIC to maintain an overview of how the individual component designs work together both electrically and in terms of physical layout. The receiver MMIC preferably occupies an area in the region of $15mm^2$, or less, for example $14.5mm^2$.

When the receiver front end further comprises a doubler/buffer amplifier MMIC, this is preferably placed between the LO and the mixer. It preferably receives the reference signal produced by the LO, and doubles the frequency of this signal producing a new reference signal which is fed to the mixer. Such a MMIC is useful when a high frequency, e.g. 30GHz, reference signal is to be produced. LOs capable of producing such signals are available, however they do not have the power capacity required to drive the mixer. LOs producing low frequency reference signals, e.g. 15GHz, are readily available and are cheap. The power capacity of these may be sufficient to drive the mixer, or may be amplified by the MMIC to drive the mixer. The signals from these may be doubled using the doubler MMIC.

The doubler component of the doubler/buffer amplifier MMIC may introduce a loss into the signal fed through it. The MMIC therefore preferably comprises a buffer amplifier component to amplify the signal compensating for the loss introduced by the doubler component. The loss introduced maybe in the region

of 6dB, and the amplifier component on the MMIC preferably gives a gain of approximately 18dB. The buffer amplifier component may also amplify the signal from the LO to provide sufficient power in the MMIC output signal to drive the mixer.

The doubler/buffer amplifier MMIC preferably also comprises a filter component comprising two quarter wavelength open circuit stubs. These allow only the doubled frequency signal to be output from the MMIC, and suppress output of the signal received from the LO.

The doubler/buffer amplifier MMIC preferably gives an output power of greater than 13dBm over the range 32 to 40GHz from an input reference signal frequency of 16 to 20GHz and power level of 0dBm. The doubler/buffer amplifier MMIC preferably uses a pinched-off 4x30μm device operating as a half wave rectifier, and is preferably matched to enhance and extract the second harmonic portion (i.e. twice the frequency) of the input reference signal from the LO. A three stage amplifier component may be used to provide 19dB of amplification and provide 30 to 40dB of rejection of the reference signal from the LO. The doubler/buffer amplifier MMIC layout may comprise an area in the region of $5mm^2$, and may comprise a GaAs substrate. The doubler/buffer amplifier MMIC may provide a reference signal having a frequency in the range 32GHz to 40GHz, from a LO operating at 16GHz to 20GHz.

Because of the good gain characteristics of the receiver front end, the receiver as a whole, to which it is attached for use, can have a gain in the region of 100dB or more. Such gains are often required in mm-wavelength receivers to boost the low power electromagnetic wave signals received in many applications to an acceptable level.

According to a second aspect of the present invention there is provided a receiver

front end package comprising a receiver front end according to the first aspect of the invention, power supply components for the receiver front end, and connectors for the receiver and the power supply components.

The receiver package is preferably double sided allowing isolation of the electromagnetic wave receiver front end and the power supply components into separate enclosures. Connections may be made between the receiver front end and the power supply components using glass bead feedthroughs in the package floor. The MMIC or MMICs of the receiver front end are preferably placed on a receiver front end circuit board, which may have a 127μm RT Duroid 5880 substrate. The MMIC or MMICs are preferably attached onto brass backing in milled pockets in the Duroid substrate.

The noise figure of the receiver front end package is preferably in the range 5.0 to 6.0dB. The package preferably measures in the region of 40mm x 27mm x 15mm (i.e. in the region of $9cm^2$) or less than this. The small size of the package is a distinct advantage over known receiver front end packages which are much more bulky and heavy. These can have a size of 10cm x 5cm x 2cm, i.e. $100cm^2$, receiver front ends of the invention corresponds to approximately a factor of ten improvement over the prior art. The small size of the receiver front end packages of the invention enables their use in systems where space is limited, and/or systems which must be easily portable.

The power supply components preferably comprise DC biasing circuits on a circuit board. These preferably contain bias sequencing and voltage regulation for all of the bias lines of the receiver front end. This allows easier implementation of the receiver front end package as all bias voltages can be derived from only two DC supplies. A sequencing circuit is preferably included to prohibit connection of the drain supplies for the receiver front end until the gate supplies have been established. The DC circuit board are preferably

implemented on 250μm Alumina using standard thin film circuit techniques.

The connectors of the receiver front end package are preferably co-axial connectors. These may be co-axial Anritsu K-connectors. They may be connected to the receiver front end using an airline launch technique. The technique preferably allows easy insertion and removal of the receiver front end circuit board, and preferably provides a better than 20dB impedance match of the connectors with the receiver front end. The receiver front end circuit board is preferably connected to the coaxial connectors by 250μm gold tape bonds. These are preferably kept as short as possible to minimise any parasitic inductance and maintain a good impedance match. Commercially available receiver packages commonly use waveguide connectors, which can be bulky and heavy.

The receiver front end package preferably exhibits a conversion gain in the region of or greater than 24dB, image rejection in the region of or greater than 40dB and a noise figure in the region of or less than 5.5dB.

The receiver front end package may be connected to an antenna, which detects the electromagnetic waves. The antenna may be movable through a substantial angle, for example the antenna may be used in a telecoms link or a sweeping radar system. Conventional receiver front ends connected to such antennas have to be able to transmit high frequency signals through a movable joint which is difficult to achieve. The receiver front end package of the invention, because of its small size, can be mounted on the antenna or a movable component thereof and can move with the antenna. The receiver front end will convert the high frequency electromagnetic waves received by the antenna to an IF output signal. This signal is fed to subsequent components via the movable joint, but because of its decreased frequency, realisation of the movable joint is much easier.

According to a third aspect of the present invention there is provided a phased

array system comprising a plurality of receiver front ends according to the first aspect of the invention.

The phased array system may be an emitter system or a detector system. Using receiver front ends of the invention has a particular advantage in this application due to their small size in comparison to conventional receiver front ends. In phased array systems it is necessary to place the receiver front ends in closely spaced channels. The spacing of the channels is limited to half the wavelength of the signal to be detected. For example, when detecting a signal having a frequency of 30GHz (i.e. a wavelength of 10mm) the spacing of the channels is limited to 5mm. The small size of the receiver front end of the invention allows them to be used in phased array systems for detecting such signals. The receiver front ends also have reduced weight. Using multifunction MMICs in the receiver front ends also reduces detrimental effects which would be present due to parasitics from connections between single function chips. This gives tight tolerances on the phase performance of the MMICs, which is particularly advantageous to the operation of phased array systems.

According to a fourth aspect of the present invention there is provided a high data rate communications system comprising one or more receiver front ends according to the first aspect of the invention.

The invention will now be further described by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic representation of a receiver front end according to the first aspect of the invention;

Figure 2 shows the layout of the low noise amplifier of Figure 1;

Figure 3 shows the layout of the mixer of Figure 1;

Figure 4 shows the layout of the filter of Figure 1;

Figure 5 shows the layout of the intermediate frequency amplifier of Figure 1;

Figure 6 shows the overall layout of the receiver MMIC of Figure 1;

Figures 7 and 8 show radio frequency on wafer (RFOW) measurements of the receiver MMIC;

Figure 9 shows the layout of the doubler/buffer amplifier MMIC of Figure 1;

Figure 10 shows the output power of the doubler/buffer amplifier as a function of input frequency;

Figure 11 is a photograph of a receiver front end package according to the second aspect of the invention;

Figure 12 shows RF, LO and IF port matches of the receiver front end package of Figure 11;

Figure 13 shows the gain conversion and the image rejection of the receiver front end package of Figure 11, and

Figure 14 shows the noise figure measurements of the receiver front end package of Figure 11 as a function of the LO frequency.

A simplified schematic representation of an electromagnetic wave receiver front end architecture is shown in Figure 1. This comprises a multifunction receiver MMIC 1 and a multifunction doubler/buffer amplifier MMIC 2. The receiver MMIC comprises a low noise amplifier (LNA) 3, a filter 4, a mixer 5, and an intermediate frequency (IF) amplifier 6. The doubler/buffer amplifier MMIC comprises a doubler 7 and an amplifier 8. The electromagnetic wave signal to be detected is fed into the input 9 of the receiver MMIC and from there to the LNA. The output of the LNA is fed through the filter to the mixer. The doubler/buffer amplifier MMIC has an input 10 into which is fed a reference signal from a local oscillator (not shown). The reference signal is fed to the doubler 7, and the output of the doubler fed to the amplifier 8. The output signal of the amplifier is fed to the mixer. This signal and that from the filter are mixed in the mixer, resulting in an IF output signal from the mixer having the characteristics of the detected signal but lower frequency. This IF signal is fed to the IF amplifier 6, and the output of this is fed to the output 11 of the receiver MMIC. All RF design work of the MMICs was performed using Libra IV (Registered Trade Mark) and design layouts were undertaken on Wavemaker (Registered Trade Mark). Electromagnetic simulation of selected parts of the MMICs, using Sonnet EM (Registered Trade Mark), was carried out to analyse the effects of unwanted coupling at the frequencies of the input signals. The components of the two MMICs will now be described in more detail.

The layout of the LNA is shown Figure 2. This comprises the front end of the receiver MMIC and receives the electromagnetic wave signals via microstrip transmission lines (not shown). Each electromagnetic signal received by the LNA is split into two substantially symmetric signals, by a Lange coupler 20. Each of the split signals is fed into a separate amplification section 21,22 of the LNA. The two signals have a 90° phase difference. The Lange coupler is provided with a load resistor 23 of 50Ω. Any signal reflected from the output

ports of the Lange coupler due to impedance mismatch is dissipated into this resistor and is not reflected out of the LNA.

Each amplification section of the LNA uses three stages of amplification, in a balanced topology. Each stage of amplification is provided with transistors 24,25,26. The transistors are supplied by a gate bias 27 and a drain bias 28. All bias tracks, in both amplification sections, are commoned so that only single gate and drain bias connections are required. This provides ease of use of the LNA. Shunt resistors 29 are provided on each transistor gate. These provide low frequency stabilisation on each gate. A series resistor-inductor-capacitor network 30 is provided in parallel with the path of each split signal. This helps to overcome potential high frequency stability problems. Parallel feedback 31 is used across the third stage transistor 26. This helps to provide gain slope compensation and unconditional stability. The output of each amplification section is combined, using a Lange coupler 32, and the combined signal output from the LNA.

Over the frequency range 30 to 40GHz the measured gain of the LNA is 23dB ± 1dB. The Lange couplers ensure that the input and output port return losses are better than 20dB. The noise figure is approximately 3.2dB.

The layout of the mixer of the receiver MMIC is shown in Figure 3. This is used to convert the frequency of the signal output from the LNA to a lower frequency mixer output signal. The mixer comprises two diodes 40,41. These are positioned in the mixer back-to-back. The signal from the LNA is fed into the mixer via a port 42, and a reference signal is fed into the mixer from the doubler/buffer amplifier MMIC via a port 43. The mixer is a 90° balanced mixer. The reference signal and the signal from the LNA output are split with a 90° phase difference by a Lange coupler 44. One portion of each of the reference signal and the LNA signal is fed to diode 40, and the other portions of

these signals are fed to diode 41 which has its orientation reversed. Each diode mixes the reference signals and the LNA signals and produces an IF output signal, which output signals are combined in phase and fed to an output port 45 of the mixer. The output IF signal has a frequency equal to the difference in frequency of the signal from the LNA and the frequency of the reference signal. If the frequency of the signal from the LNA is 35GHz and the frequency of the reference signal is 30GHz, then the frequency of the IF signal output from the mixer will be 5GHz.

This 90° balanced mixer topology provides very good input and output port impedance matches, giving the mixer input ports a broadband 50Ω impedance. The mixer preferably has a conversion loss of less than 10dB, LNA and reference signal input port return losses of greater than 15 dB and LO-RF isolation (i.e. isolation of the LO or reference signal from the signal from the LNA)of greater than 6dB. The LO-IF isolation (i.e. the amount of the reference signal seen in the (IF) output signal of the mixer) is greater than 15dB.

Prior to being fed to the mixer, the output signal from the LNA is fed through a filter. The layout of the filter is shown in Figure 4. This comprises a distributed transmission line design. To reduce MMIC area the filter is folded into a serpentine layout. The filter comprises five elements 50, which are quarter-wave coupled.

The passband of the filter is such that it suppresses a lower sideband. The passband of the filter is 35 to 40GHz. This will suppress a lower sideband of 25GHz, allowing only the 35GHz sideband to be output from the filter. The filter produces a stopband attenuation of 49dB at 25GHz. The passband insertion loss of this filter is in the region of 2.3dB from 35 to 40GHz, and the port impedance matches are better than 15dB.

The layout of the IF amplifier is shown in Figure 5. This receives the IF output signal from the mixer and amplifies it producing an IF output signal which is output from the receiver MMIC. The IF amplifier comprises a single transistor stage 60, and has a gain of greater than 9dB. A 400μm gate width transistor 60 capable of delivering 15dBm of output power is used for this amplifier. This avoids the IF amplifier compressing before the LNA. The transistor is connected to a gate bias 61 and a drain bias 62. A parallel resistor-inductor-capacitor feedback network 63 is applied between the gate and drain bias terminals of the transistor. This helps to reduce the sensitivity of the IF amplifier to process variations. The IF amplifier input presents a 50Ω impedance to the mixer at mm wavelengths as well as at IF frequencies. This helps to ensure correct mixer operation.

An RC network 64 is provided on the input to the IF amplifier. This is designed to ensure that an input impedance of 50 ohms is presented to the mixer output over a frequency range of DC to 50GHz. This helps to provide a good termination at the LO and RF frequencies in the mixer to ensure low RF and LO breakthrough and thus maintain good RF-IF and LO-IF isolation.

Figure 6 shows the overall layout of the receiver MMIC showing the LNA 70, the filter 71, the mixer 72 and the IF amplifier 73. The MMIC has a size of 5.5mm x 2.64mm. Radio frequency on wafer (RFOW) measurements of the receiver MMIC are shown in figures 7 and 8. With a 32GHz, 11dBm reference signal and an IF output signal of 5GHz the receiver MMIC exhibits 25dB conversion gain, approximately 40dB image rejection, 3.5dB noise figure and P1dB of 14dBm. The receiver MMIC is capable of receiving electromagnetic wave signals having frequencies in the range 35 to 40GHz or greater than this.

The layout of the doubler/buffer amplifier MMIC is shown in Figure 9. This is placed between the LO and the mixer. It receives the reference signal produced

by the LO via input port 81, and doubles the frequency of this signal using a doubling component 82. The signal from this is then fed to a series of amplification stages 83 which produce a new reference signal which is output from the MMIC via output port 84. The doubler/buffer amplifier stages use a pinched-off 4x30μm device operating as a half wave rectifier, and are matched to enhance and extract the second harmonic of the signal from the LO. Three stages of amplification are used to provide 13dB of amplification and provide 30 to 40dB of rejection of the LO signal. The doubler/buffer amplifier MMIC also comprises a filter component comprising two quarter wavelength open circuit stubs 85. These allow only the doubled frequency signal to be output from the MMIC, and suppress output of the signal received from the LO. The doubler/buffer amplifier MMIC layout has an area of approximately 4.7mm^2 .

Measured RFOW results from the doubler MMIC are shown in figure 10. For an input power of +1dBm, ≥11dBm output power was obtained over the 32 to 40GHz frequency range. By increasing the input power to +6dBm, typically 15 to 16dBm of output power was obtained, more than enough to drive the mixer. Rejection of the LO signal was measured better than 28dB over the same band.

A photograph of a receiver front end package is shown in Figure 11. This comprises a receiver front end and power supply components for the receiver front end. The receiver package is double sided allowing isolation of the electromagnetic wave receiver front end and the power supply components into separate enclosures. Connections are made between the receiver front end and the power supply components using glass bead feedthroughs in the package floor. The MMICs of the receiver front end are placed on a receiver front end circuit board, which has a 125μm RT Duroid 5880 substrate. The MMICs are attached onto brass backing in milled pockets in the Duroid substrate.

The noise figure of the receiver front end package is in the range 5.0 to 6.0dB.

The package measures in the region of 40mm x 27mm x 15mm (i.e. in the region of 9cm^2) or less than this. The power supply components comprise DC biasing circuits on a circuit board. These contain bias sequencing and voltage regulation for all of the bias lines of the receiver front end. This allows easier implementation of the receiver front end package as all bias voltages can be derived from only two DC supplies. A sequencing circuit is included to prohibit connection of the drain supplies for the receiver front end until the gate supplies have been established. The DC circuit board are implemented on 250μm Alumina using standard thin film circuit techniques.

The connectors of the receiver front end package are co-axial Anritsu K-connectors, connected to the receiver front end using an airline launch technique. The technique allows easy insertion and removal of the receiver front end circuit board, and provides a better than 20dB impedance match of the connectors with the receiver front end. The receiver front end circuit board is connected to the coaxial connectors by 250μm gold tape bonds. These are kept as short as possible to minimise any parasitic inductance and maintain a good impedance match. The receiver front end package exhibits a conversion gain in the region of or greater than 24dB, image rejection in the region of or greater than 40dB and a noise figure in the region of or less than 5.5dB.

When the receiver front end package is used to downconvert a 36.9GHz RF input signal to a 6GHz IF output signal, an LO input of 15.45GHz, doubled to 30.9GHz, was required. This meant that the doubler/buffer amplifier MMIC was being operated at the lower limit of its bandwidth and therefore had to be supplied with 8dBm to provide enough output power to drive the mixer. Figure 12 shows RF (LNA signal), LO (reference signal) and IF port matches of the package to be better than 10dB. Small signal gain is shown in figure 13 to be greater than 24dB over an IF range of 2.5 to 8.5GHz. Image rejection at 6GHz IF was measured at 43.4dB. Noise figure measurements were carried out on the

receiver front end package and are shown in figure 14 at a fixed IF of 6GHz with the LO swept from 35.9 to 37.9GHz. It can be seen that the noise figure of the complete package is typically 5.0 to 6.0dB (±0.5dB uncertainty in the measurement).

CLAIMS

1. A receiver front end capable of receiving electromagnetic wave signals having frequencies in the range of substantially 35GHz to substantially 40GHz, and having a gain of substantially 24dB or above and a noise figure of substantially 4dB or below, and comprising one or more multifunction monolithic microwave integrated circuits (MMICs).

2. A receiver front end according to claim 1 which has a noise figure of substantially 4dB or below over an output signal frequency range of substantially 1 to 10GHz.

3. A receiver front end according to any preceding claim in which the or each multifunction receiver front end MMIC carries out a plurality of functions and the functions comprise amplification of the electromagnetic wave signals received by the MMIC, and/or filtering the electromagnetic wave signals, and/or conversion of the frequency or frequencies of the electromagnetic wave signals to a lower or higher frequency or frequencies, and/or amplification of the converted signals.

4. A receiver front end according to any preceding claim which comprises a receiver MMIC and a doubler/buffer amplifier MMIC, and in which the receiver MMIC comprises a low noise amplifier (LNA), with a noise figure less than 4dB.

5. A receiver front end according to claim 4 in which the LNA is a balanced amplifier, and each electromagnetic signal received by the LNA is split into two substantially symmetric signals, each of which is fed into a separate amplification section.

6. A receiver front end according to claim 5 in which each amplification section of uses three stages of amplification, and the output of each amplification section is combined and the combined signal output from the LNA.

7. A receiver front end according to any of claims 4 to 6 in which the receiver MMIC comprises a mixer, and in which the mixer converts the frequency of a signal output from the LNA to a lower frequency mixer output signal.

8. A receiver front end according to claim 7 in which the mixer comprises two diodes and the signal from the LNA is fed into the diodes along with a reference signal and the diodes multiply the signal from the LNA and the reference signal and output a signal having a frequency equal to the difference in frequency of the signal from the LNA and the frequency of the reference signal.

9. A receiver front end according to any of claims 7 to 8 in which the mixer is a 90° balanced mixer.

10. A receiver front end according to any of claims 4 to 9 in which the receiver MMIC comprises a filter, and the filter is placed between the LNA and the mixer, to filter the signal from the LNA before it is fed to the mixer.

11. A receiver front end according to claim 10 in which the passband of the filter is such that it suppresses a sideband of the signal from the LNA.

12. A receiver front end according to any of claims 10 to 11 in which the filter comprises a distributed transmission line design, in which the filter is folded into a serpentine layout.

13. A receiver front end according to any of claims 4 to 12 in which the

receiver MMIC comprises an IF amplifier, and the IF amplifier receives an IF output signal from the mixer and amplifies it producing an IF output signal which is output from the receiver MMIC.

14. A receiver front end according to claim 13 in which the amplifier comprises a single transistor stage, and in which a parallel resistor-inductor-capacitor feedback network is applied between the gate and drain terminals of the transistor.

15. A receiver front end according to any of claims 4 to 14 in which the doubler/buffer amplifier MMIC is placed between the LO and the mixer, and the doubler/buffer amplifier MMIC receives the reference signal produced by the LO, and doubles the frequency of this signal producing a new reference signal which is fed to the mixer.

16. A receiver front end according to claim 15 in which the doubler/buffer amplifier MMIC comprises a filter component comprising two quarter wavelength open circuit stubs.

17. A receiver front end package comprising a receiver front end according to any of claims 1 to 16, power supply components for the receiver front end, and connectors for the receiver and the power supply components.

18. A receiver front end package according to claim 17 which is double sided allowing isolation of the electromagnetic wave receiver front end and the power supply components into separate enclosures, and in which connections are made between the receiver front end and the power supply components using glass bead feedthroughs in the package floor.

19. A receiver front end package according to any of claims 17 to 18 in which

the power supply components comprise DC biasing circuits on a circuit board, and in which the biasing circuits contain bias sequencing and voltage regulation for all of the bias lines of the receiver front end.

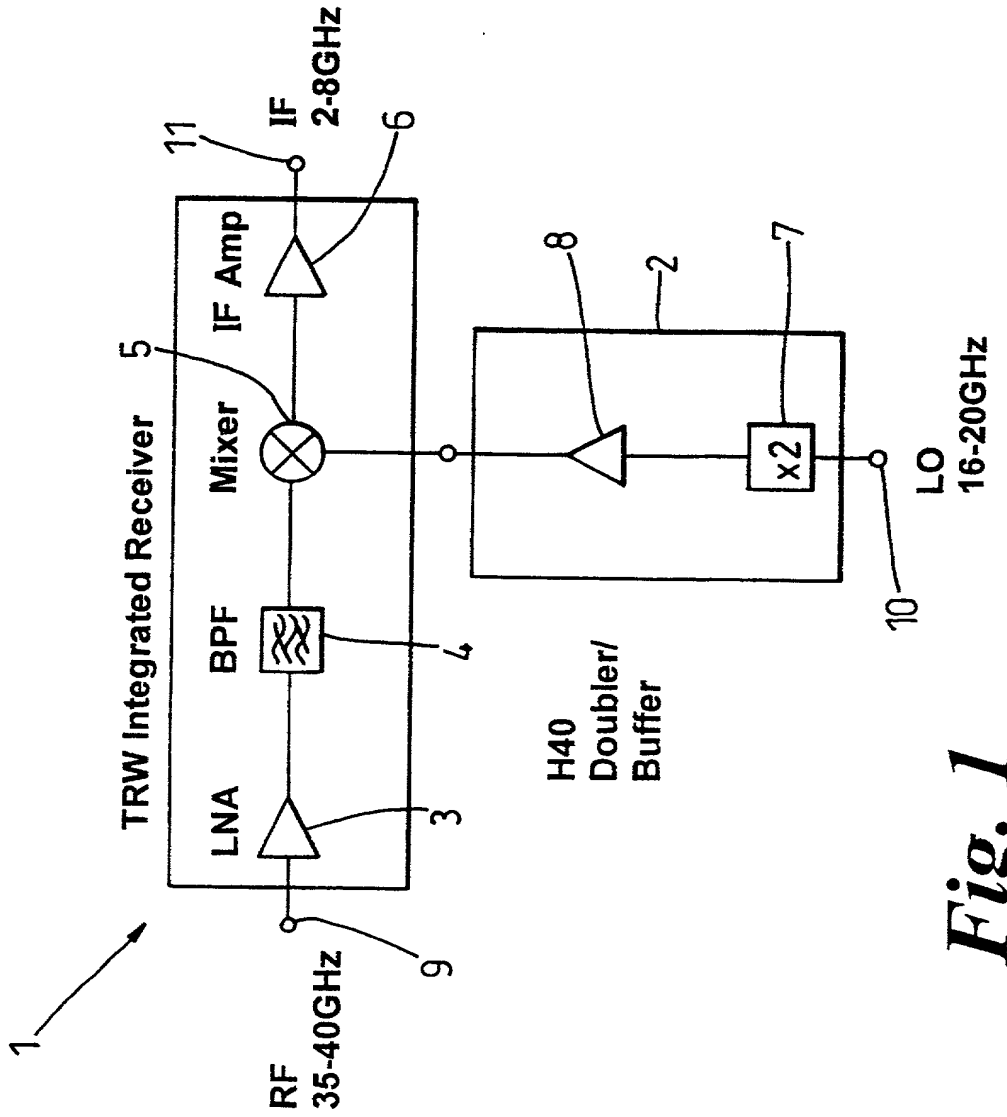
20. A receiver front end package according to claim 19 in which the connectors are connected to the receiver front end using an airline launch technique, which allows easy insertion and removal of the receiver front end, and provides a better than 20dB impedance match of the connectors with the receiver front end.

21. A receiver front end package according to any of claims 17 to 20 in which the receiver front end package is connected to an antenna, which detects the electromagnetic waves.

22. A receiver front end package according to claim 21 in which the receiver front end package is mounted on the antenna or a movable component thereof and can move with the antenna.

23. A phased array system comprising a plurality of receiver front ends according to any of claims 1 to 16.

24. A high data rate communications system comprising one or more receiver front ends according to any of claims 1 to 16.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BPF
Mixer
IF Amp
IF
2-8GHz
RF
35-40GHz
H40
Doubler/
Buffer
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3
4
5
6
7
8
9
10
11

Fig. 1

2/10

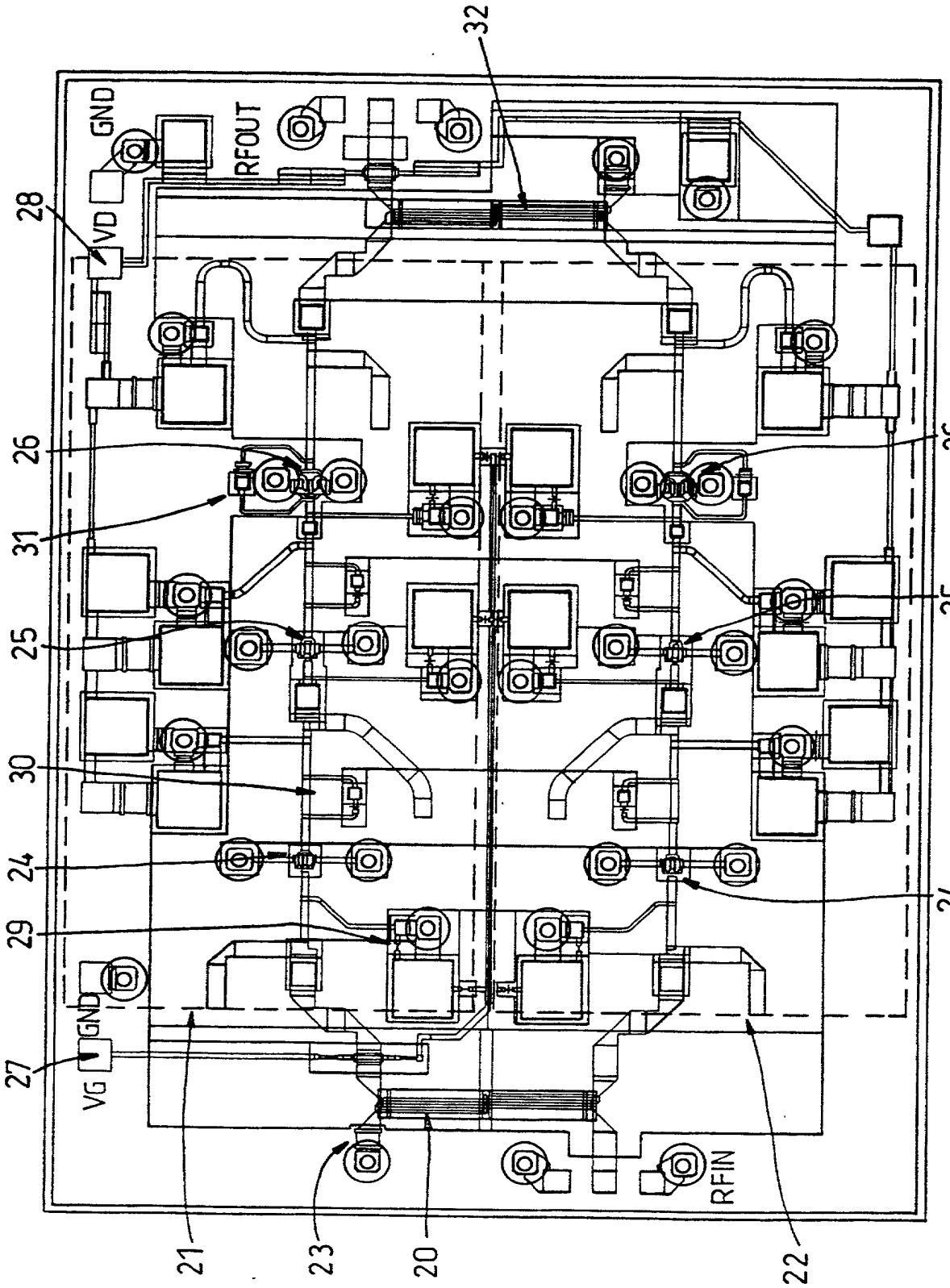
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Fig. 2

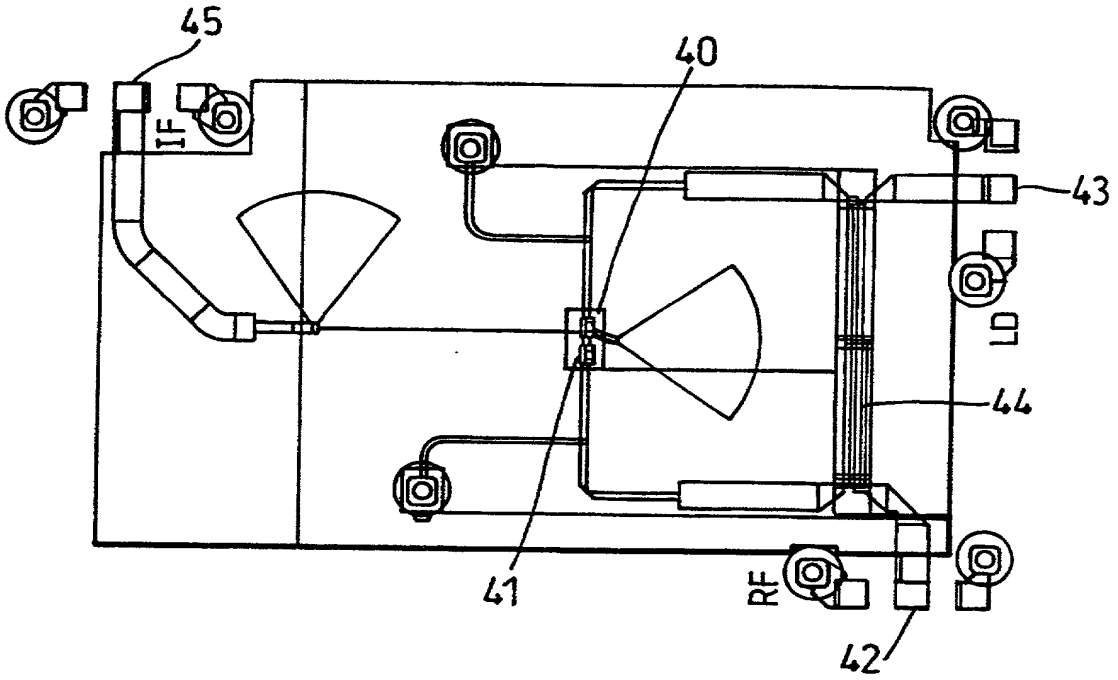


Fig. 3

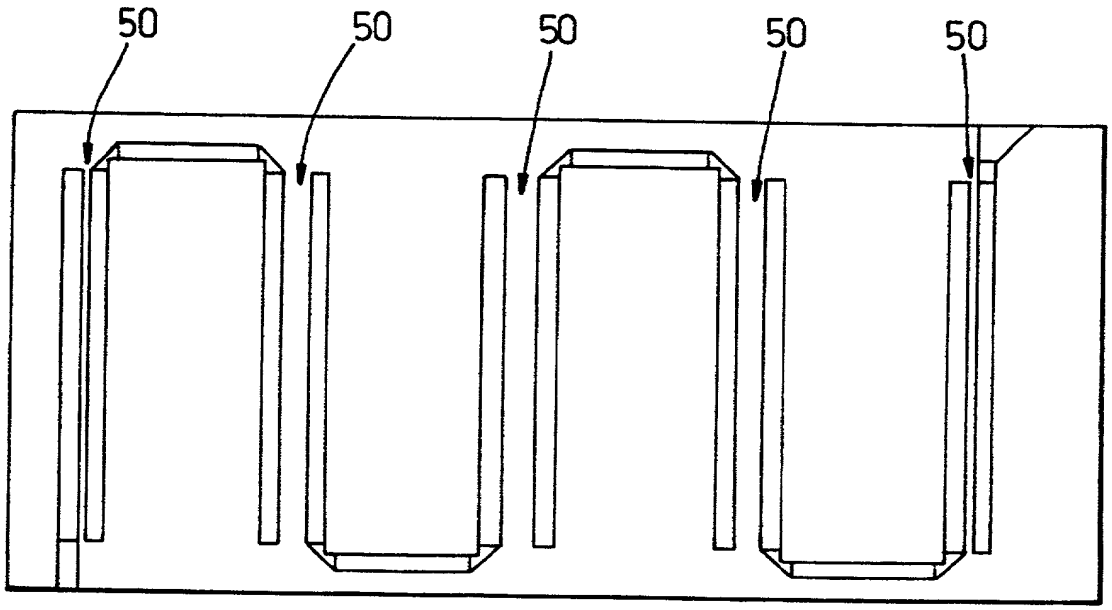


Fig. 4

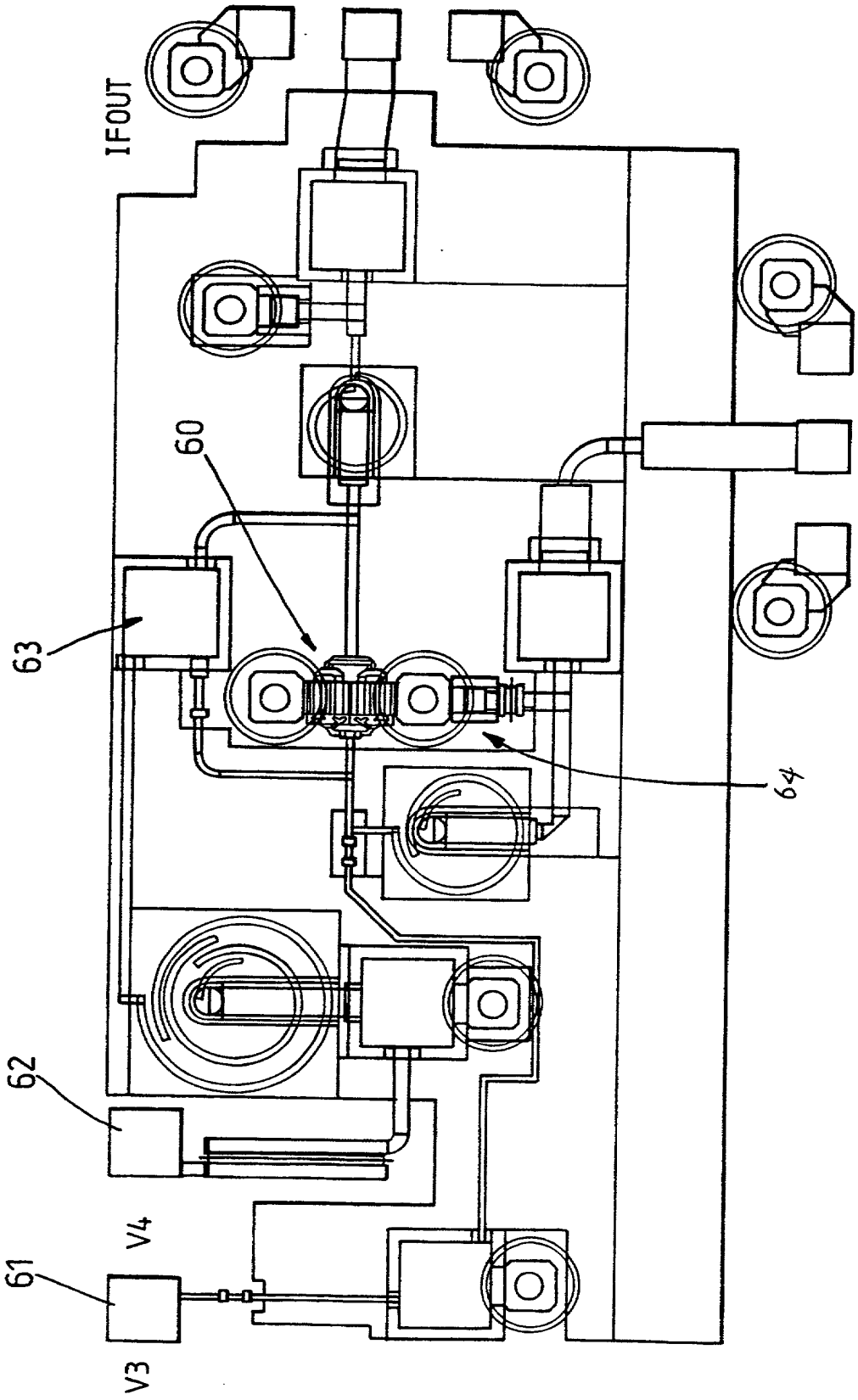


Fig. 5

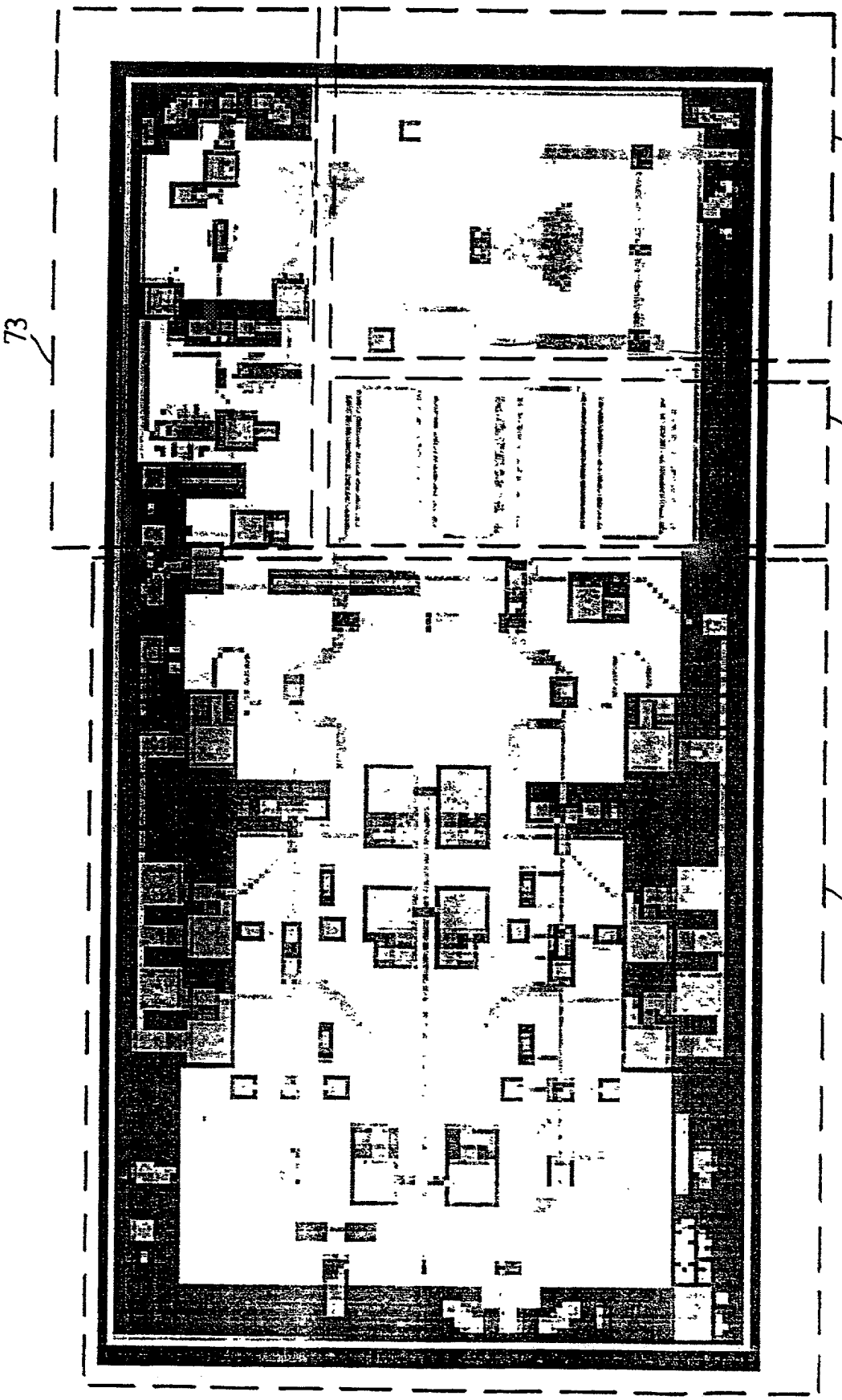
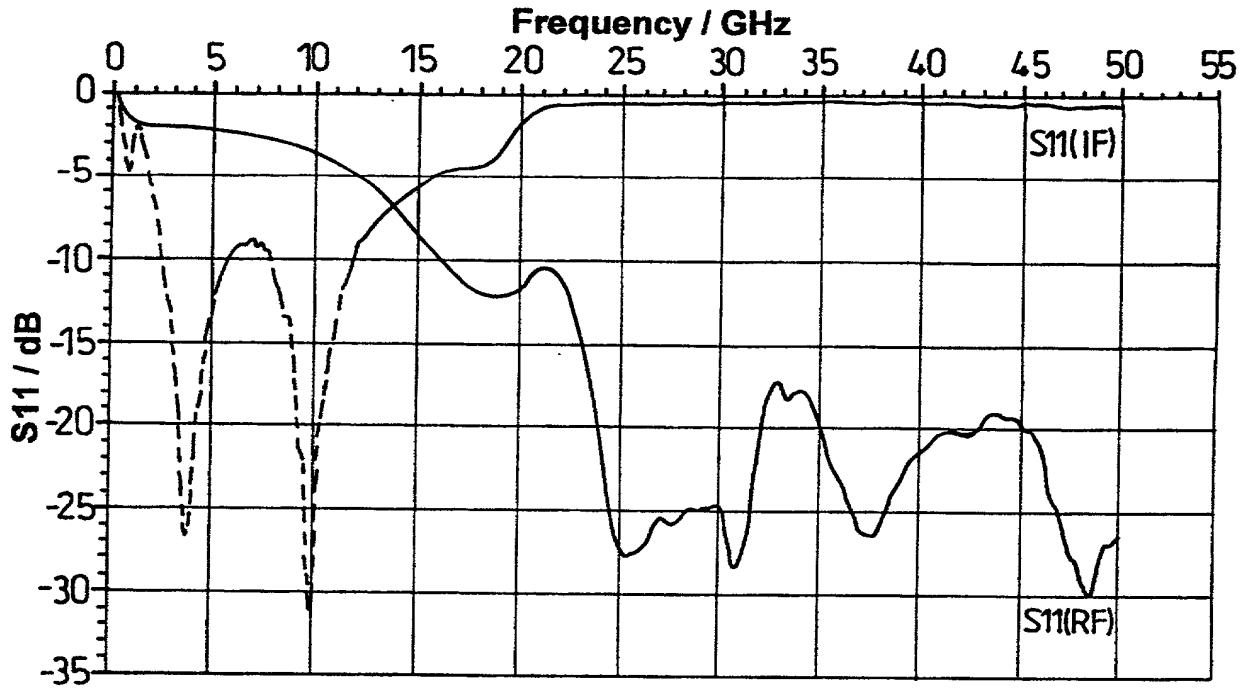


Fig. 6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20
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30
35
40
45
50
55
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-30
-35
S11 / dB
S11(IF)
S11(RF)

Fig. 7

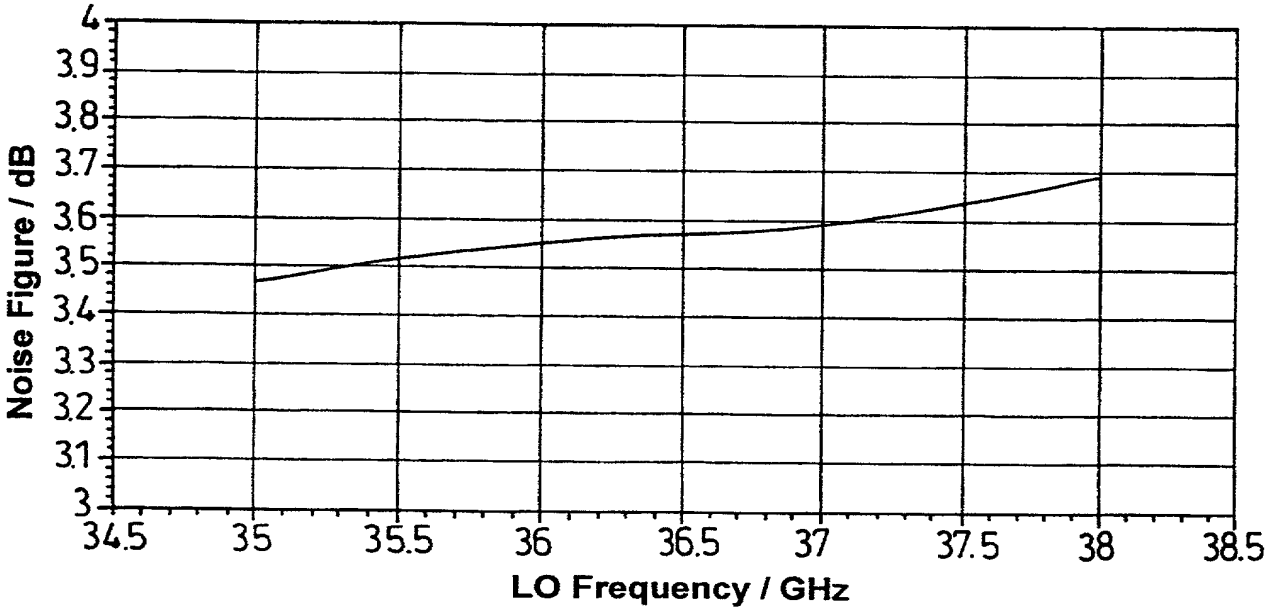
4
3.9
3.8
3.7
3.6
3.5
3.4
3.3
3.2
3.1
3
Noise Figure / dB
34.5
35
35.5
36
36.5
37
37.5
38
38.5
LO Frequency / GHz

Fig. 8

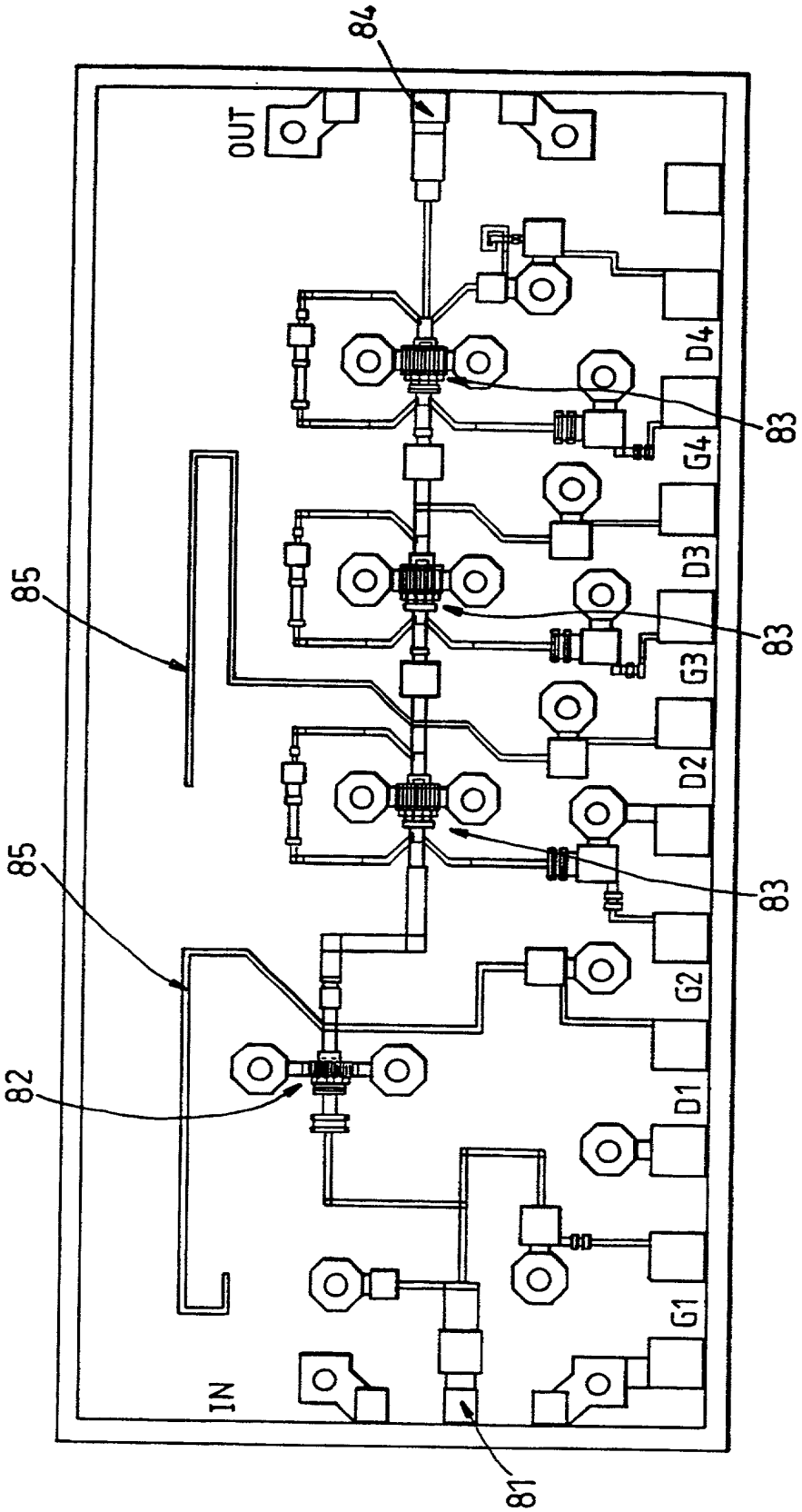

Fig. 9

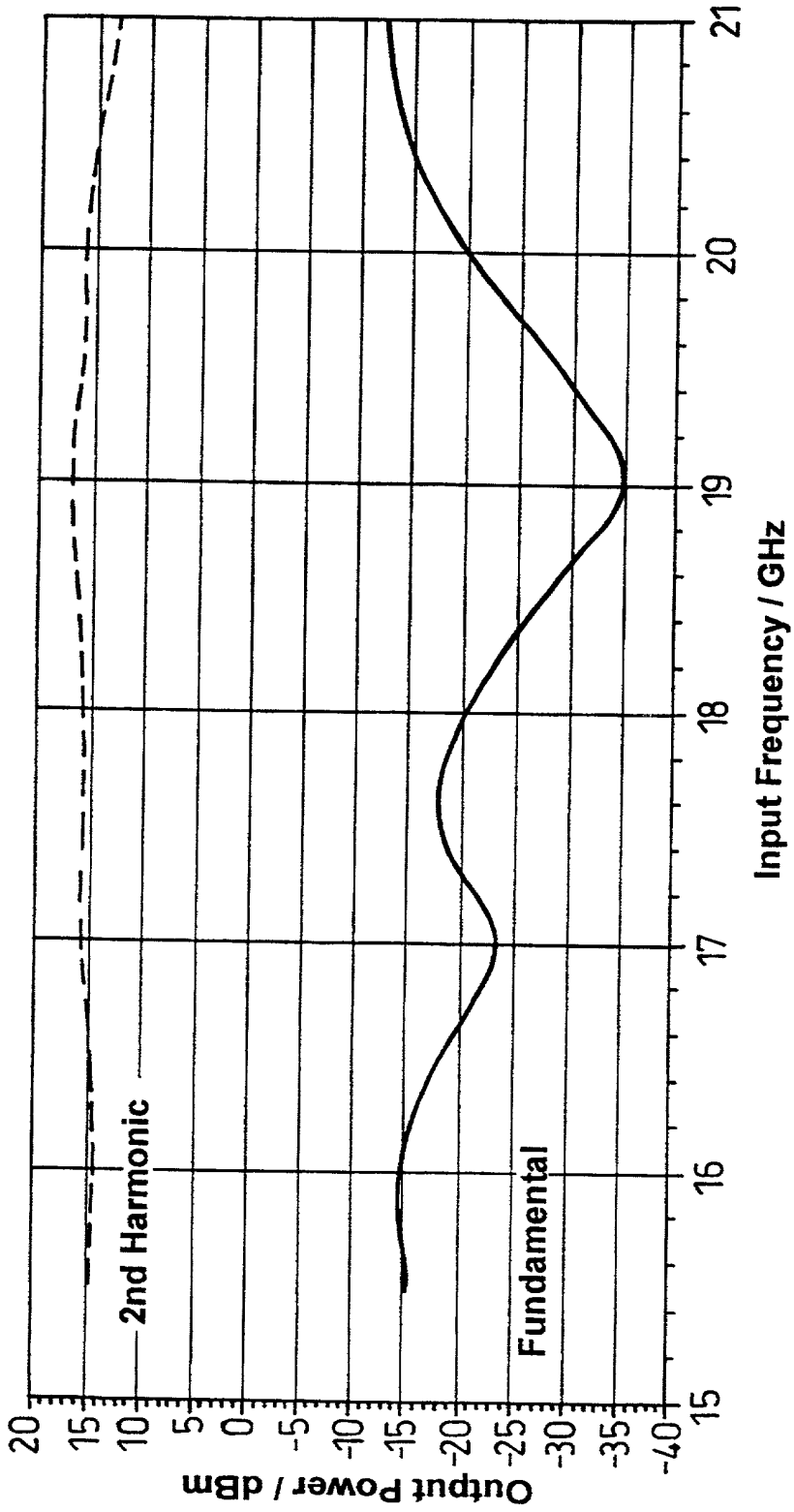
Output Power / dBm
20
15
10
5
0
-5
-10
-15
-20
-25
-30
-35
-40
15
16
17
18
19
20
21
Input Frequency / GHz
2nd Harmonic
Fundamental

Fig. 10

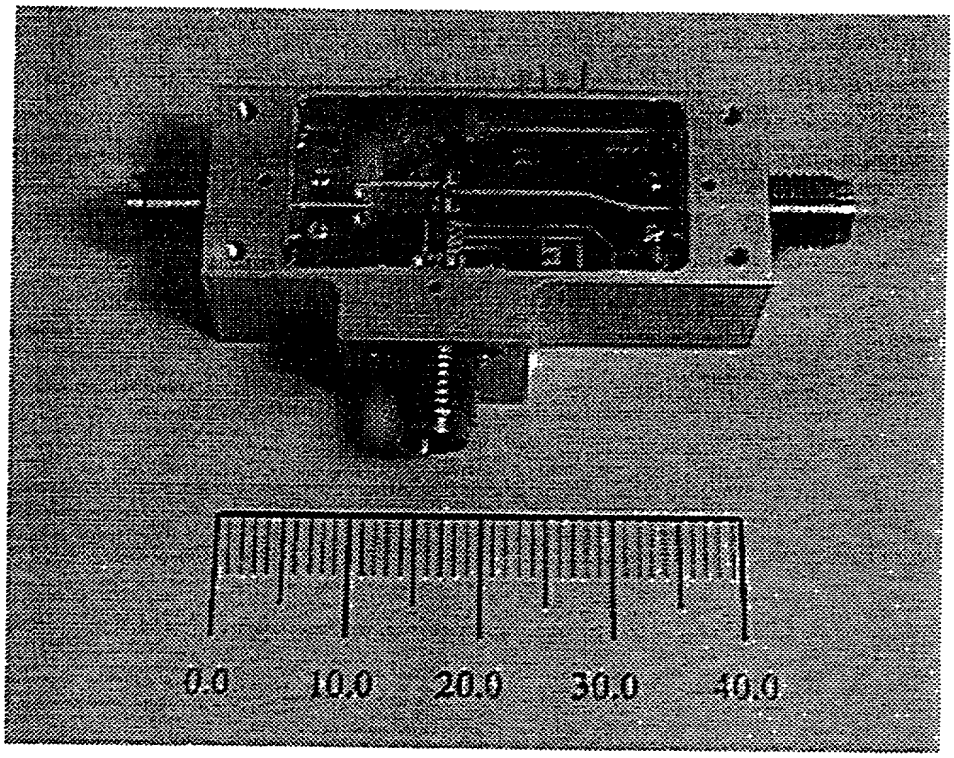
0.0
10.0
20.0
30.0
40.0

Fig. 11

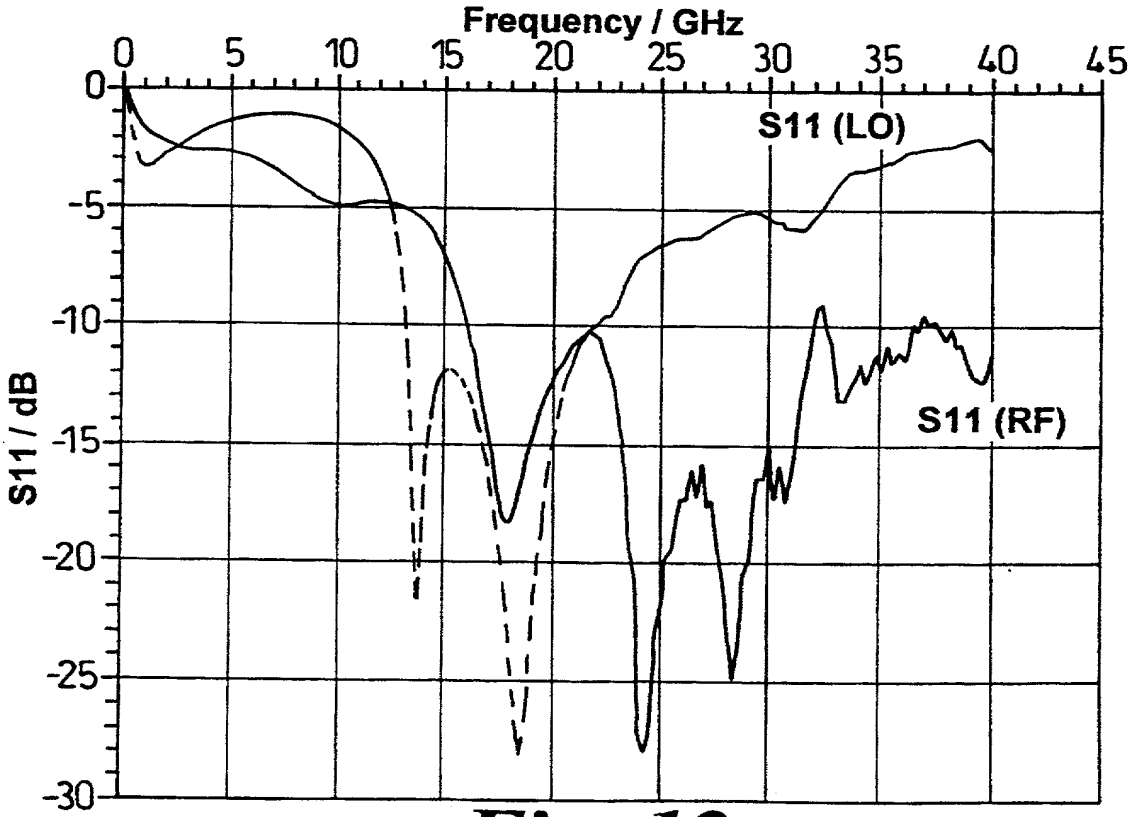
Frequency / GHz
0
5
10
15
20
25
30
35
40
45
S11 / dB
0
-5
-10
-15
-20
-25
-30
S11 (LO)
S11 (RF)

Fig. 12

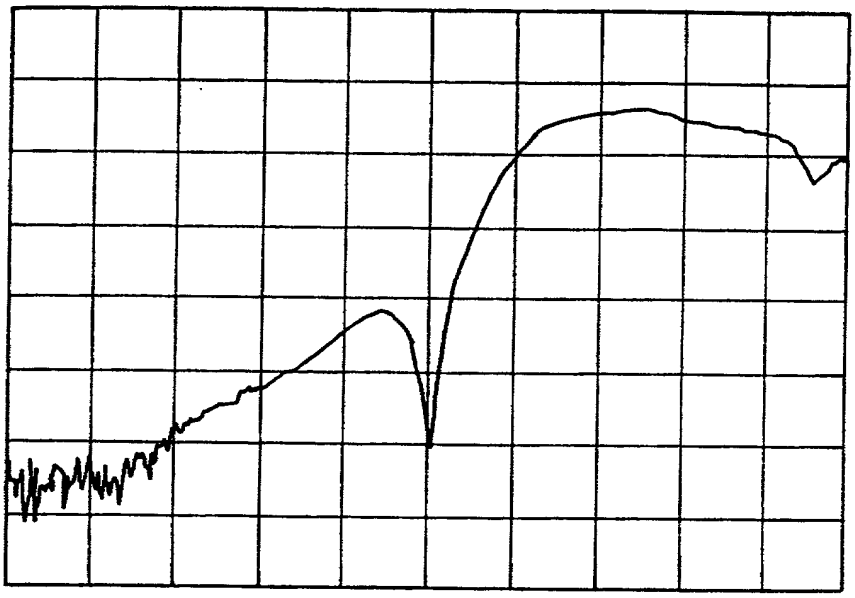

Fig. 13

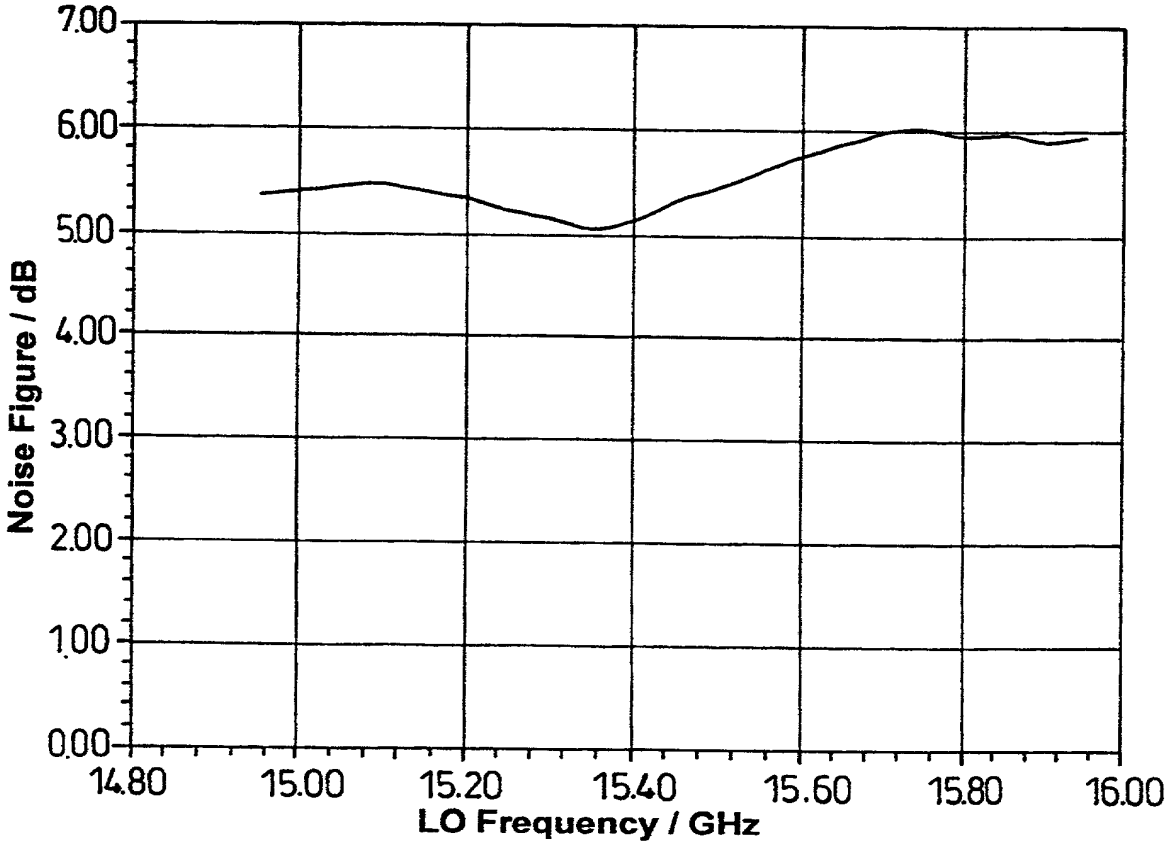
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
Noise Figure / dB
14.80
15.00
15.20
15.40
15.60
15.80
16.00
LO Frequency / GHz

Fig. 14

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1. Inventor's Signature: P.D. Munday Date: 15th November 2001.
Inventor: Paul (first) D. (MI) MUNDAY (last) British (citizenship)
Residence: (city) Malvern (state/country) Worcestershire, England GBX
Mailing Address: DERA Malvern, St. Andrews Road, Malvern, Worcestershire, England
(Zip Code) WR14 3PS

2. Inventor's Signature: A. R. Barnes Date: 20TH NOVEMBER 2001
Inventor: Andrew (first) R. (MI) BARNES (last) British (citizenship)
Residence: (city) Malvern (state/country) Worcestershire, England GBX
Mailing Address: DERA Malvern, St. Andrews Road, Malvern, Worcestershire, England
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3. Inventor's Signature: _____ Date: _____
Inventor: ~~Geoffrey~~ (first) MI BALL (last) British (citizenship)
Residence: (city) Malvern (state/country) ~~Worcestershire~~, England GBX
Mailing Address: DERA Malvern, St. Andrews Road, Malvern, Worcestershire, England
(Zip Code) WR14 3PS

4. Inventor's Signature: _____ Date: _____
Inventor: Mark (first) T. MI MOORE (last) British (citizenship)
Residence: (city) Wigston (state/country) Leicester, England GBX
Mailing Address: 27 Ruskington Drive, Wigston, Leicester, England
(Zip Code) LE18 1LB

5. Inventor's Signature: [signature] Date: 15th November 2001
Inventor: Alexander (first) L. MI BROWN (last) British (citizenship)
Residence: (city) North Finchley (state/country) London, England GBX
Mailing Address: 9 Brittania Road, North Finchley, London, England
(Zip Code) N12 9RU

FOR ADDITIONAL INVENTORS, check box ☐ and attach sheet with same information and signature and date for each.

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Mailing Address: DERA Malvern, St. Andrews Road, Malvern, Worcestershire, England
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3. Inventor's Signature: G. Ball Date: 14 February 2002
Inventor: Geoffrey (first) | MI | BALL (last) | British (citizenship)
Residence: (city) Malvern (state/country) Worcestershire, England
Mailing Address: DERA Malvern, St. Andrews Road, Malvern, Worcestershire, England
(Zip Code) WR14 3PS

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Inventor: Mark (first) | T. MI | MOORE (last) | British (citizenship)
Residence: (city) Wigston (state/country) Leicester, England
Mailing Address: 27 Ruskington Drive, Wigston, Leicester, England
(Zip Code) LE18 1LB

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P2825

124-889
JL3065

Nixon & Vanderhye P.C. (10/98)
(Domestic Non-Assigned/Foreign) Page 1

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RULE 63 (37 C.F.R. 1.63)
INVENTORS DECLARATION FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, mailing address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ELECTROMAGNETIC WAVE RECEIVER FRONT END

the specification of which (check applicable box(s)):

☐ is attached hereto
☐ was filed on _____ as U.S. Application Serial No. _____ (Atty Dkt. No. 124-859)
☒ was filed as PCT International application No. PCT/GB00/00953 on 15 March 2000
and (if applicable to U.S. or PCT application) was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose to the Patent Office all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	Country	Day/Month/Year Filed
9906047.7	Great Britain	17 March 1999

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	Date/Month/Year Filed

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed above or below:

Prior U.S./PCT Application(s): Application Serial No.	Day/Month/Year Filed	Status: patented pending, abandoned
PCT/GB00/00953	15 March 2000	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. And on behalf of the owner(s) hereof, I hereby appoint **NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 8th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed)**, and the following attorneys thereof (of the same address) individually and collectively owner's/owners' attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Larry S. Nixon, 25640; Arthur R. Crawford, 25327; James T. Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E. Nusbaum, 32348; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Jeffry H. Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr. 29366; Mary J. Wilson, 32955; J. Scott Davidson, 33489; Alan M. Kagen, 36178; Robert A. Molan, 29834; B. J. Sadoff, 36663; James D. Berquist, 34776; Updeep S. Gill, 37334; Michael J. Shea, 34725; Donald L. Jackson, 41090; Michelle N. Lester, 32331; Frank P. Presta, 19828; Joseph S. Presta, 35329; Joseph A. Rhoa, 37515; Raymond Y. Mah, 41426; Chris Comuntzis, 31097; Gary T. Tanigawa, 43180. I also authorize Nixon & Vanderhye to delete any attorney names/numbers no longer with the firm and to act and rely solely on instructions directly communicated from the person, assignee, attorney, firm, or other organization sending instructions to Nixon & Vanderhye on behalf of the owner(s).

3. Inventor's Signature: _____ Date: _____
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5. Inventor's Signature: _____ Date: _____
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FOR ADDITIONAL INVENTORS, check box ☐ and attach sheet with same information and signature and date for each.